Fabrication Guidelines

Arlon DiClad, CuClad, IsoClad and AD Series Laminates

Arlon's PTFE laminates are fiberglass reinforced PTFE resin-based composites. Primary application of these products is their specification and use as printed circuit substrates for higher frequency applications, where low loss and controlled dielectric constant are required. Applications include, but are not limited to filters, couplers, low noise amplifiers, power dividers and combiners. By controlling PTFE resin to fiberglass ratio, Arlon is able to offer a range of products from very low dielectric constant and dissipation factor to more highly reinforced laminate with better dimensional stability.

Arlon PTFE materials used in stripline or microstrip applications can be fabricated using mostly conventional board fabrication processes and techniques. These materials can be processed with certain adjustments to machining parameters and a few in-line modifications.

Processing Guidelines for DiClad, CuClad, Isoclad and AD Series Materials

Storage:	Store material flat in a cool, dry area, away from direct sunlight. Avoid copper oxidation and material contamination.
Bonding:	Stripline or Buried Microstrip bonding can be accomplished using Arlon's CuClad® 6700 Bonding Film or CuClad® 6250 Bonding Film, or other prepregs or adhesives which support electrical performance requirements. Copper oxide treatments can may used when bonding with FR-4 prepregs (especially on a full ground plane). For either bonding film, good results are achieved when bonding directly fo lows copper etching (and drying). Adhesion to the laminate surface can be improved with sodium o plasma etch prior to bonding. Adhesion to the copper surface can be improved with a micro-etch prior to bonding. Contact Arlon for process parameters for use with either CuClad 6700 Bonding Film or CuClad 6250 Bonding Film. In the case of mixed-material multilayer constructions, it may be specified to use FR-4 prepregs, especially where RF functions are isolated by a full ground plane. Copper oxide treatment recommendations from the prepreg manufacturer are suggested for use with their product. CuClad 6700 Bonding Film has a higher melt temperature than many prepregs require for cure. In mixed-material multilayer constructions it may be necessary to perform sequential lamination. Bonding film melt temperature and prepreg cure temperature should be among considerations when selecting.
Dimensional Stability:	Dimensional stability depends on dielectric thickness, resin to glass ratio, copper foil thickness and how much copper is retained (specific to each PCB design). That is, designs having significant ground planes will have less shrinkage upon etching the copper away. Dimensional stability may be improved by baking for 1 hour at 300°-310°F (150°-155°C) and cooling slowly, prior to establishing a pattern for registration. Mechanical scrubbing puts the conductor-dielectric interface under stress and contribute to poor dimensional stability, In some multilayer work, it is common with FR-4 prepreg to use solid copper fill and borders. However, solid borders on inner layers may impact flow of low loss, low dielectric constant adhesives for lamination of multilayer PTFE-based constructions.

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Drilling:

Drill PTFE materials using highly polished, new carbide tools (not re-points). More recent investigation finds Diamond Coated and Diamond-Like Coated bits are also very effective. In some cases, panels may be drilled in stacks, based on total thickness (and resulting aspect ratio). Use of rigid entry (.020"-.030") and exit (.060"-.093") material is recommended. The following feeds and speeds are recommended as a starting point and specific process parameters can be refined (exploration of lower parameters are often used with smaller diameter bits).

Chip load: 0.002-0.003 inch/revolution
Surface speed: 400-450 surface feet/minute
Retract rate: 500-600 inch/minute
Tool life: 500-1000 hits (depending on stack height)hip load: 0.002-0.003 inch/revolution
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Deburring:

Optimization of drilling should include a goal for eliminating the need for aggressive deburring. If deburring is necessary, properly support the back side of the panel and apply light circular motion with wet 600 grit sandpaper. Use a high pressure spray to remove loose debris in the holes. Mechanical deburring can affect dimensional stability, as described with mechanical scrubbing.

Hole Wall Preparation:

Hole wall resin activation is typically necessary for PTFE-based laminates to ensure coverage with electroless copper deposition. This can be done with plasma or sodium etchants. The following is an example of one plasma cycle for PTFE materials:

Process Step	**Gas Mixture**	**Time/Power**
Heat-up	O_2/20% N_2	To reach 70-90˚C Material temp
Surface Etch	H_2 / 20% N_2 or N_2 / 20% O_2	30 minutes @ 75% of full power
O_2 Burn	O_2/100%	5 min at 50% power to remove residue

Holding time following plasma treatment is limited. The plasma process should be repeated if hold time extends beyond 12 hours. For additional information on plasma treatment for PTFE please visit **www.arlon-med.com.**

Commercially available sodium etchants are commonly used. Please contact the following supplier to obtain processing guidelines for their products:

Action Technologies, Inc. www.actontech.com Telephone: 570-654-0612 Product FluoroEtch®

PTFE Fabrication Guidelines (cont.)

Surface Prep:	Bake for 90 minutes at 110°C after sodium etch treatment. Standard chemical cleaning techniques are recommended for cleaning copper. Mechanical scrubbing is not recommended for PTFE-based materials; dimensional changes occur when force is applied to copper surfaces.
Copper Plating:	Following plasma or sodium treatment as described above, conventional electroless deposition or direct plate copper may be used along with conventional electrolytic copper plating.
Etching:	Conventional ammoniacal or cupric etchants may be used to remove unwanted copper. Rinse thoroughly with warm water after processing.
Resist Strip:	Conventional resist strippers may be used to remove unwanted resist.
Soldermask:	For SMOBC parts, it is recommended to apply solder mask coating within 12 hours after copper etching for best adhesion. For solder mask adhesion to exposed dielectric, sodium or plasma etch will improve bond to the laminate surface; a micro-etch may be used to improve the copper surface. Where either wet etch process is used, bake PTFE materials following rinse for one hour at 225°-250°F (110°-120°C) to remove residual moisture before solder mask processing.
Solder Leveling:	Bake PTFE materials for 1-2 hours at 225°-250°F (110°-120°C) prior to solder leveling. It is recommended boards are racked (vertically, if possible) to ensure proper air circulation around parts to fully dissipate residual moisture. Be aware some PTFE laminates have high z-axis expansion and high temperature exposure may result in barrel cracks. Plated through holes should have 2 mil minimum wall thickness for low DK laminates which require HAL.
Electroless Gold:	It is important to employ adequate rinse procedures, according to chemical vendors' process guidelines, to ensure reliable yield through chemical plating.
Routing:	It is recommended to use commercially available, two-flute, slow spiral, micro-grain carbide, upcut, endmill bits. Support PTFE products with rigid entry and back-up materials. It is important to exert sufficient clamping pressure through the router foot to prevent the material stack it from being pulled up from the table.. Typical rout parameters for an 0.062" cutting tool: Spindle Speed: 15,000 rpm Table Feed Rate: 15 inches/minute

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